

WHAT IS CLAIMED IS:

1. An integrated circuit device package (10), comprising:

an integrated circuit device (12) having an electrically active surface (16) and an opposing backside surface (14) and sides (17) extending therebetween, said electrically
5 active surface (16) having a plurality of electrically active circuit traces formed thereon and metallized bumps (18) extending from selected sites on said circuit traces;

a plurality of electrically conductive leads (20) each having respective first surfaces and opposing second surfaces;

10 a plurality of electrical contacts (24) extending outward from said respective first surfaces;

a solder (22) electrically and mechanically bonding said metallized bumps (18) to said second surfaces; and

15 a dielectric molding resin (26) formed into a package at least partially encapsulating said integrated circuit device (12) and said plurality of electrically conductive leads (20), said backside surface (14) and said plurality of electrical contacts (24) are exposed on opposing sides of said package.

2. The package (10) of claim 1 wherein said sides (17) include at least one feature that is effective to limit the ingress of moisture along an interface between said integrated
20 circuit device (12) and said dielectric molding resin (26).

3. The package (10) of claim 2 wherein said at least one feature includes two elements (58, 60) that intersect at an angle of approximately 90°.

25 4. The package (10) of claim 2 wherein a thickness of said package (10) is less than three times a thickness of said integrated circuit device (12).

5. The package (10) of claim 4 wherein said thickness of said package (10) is approximately 0.01 inch.

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6. The package (10) of claim 2 wherein said integrated circuit device (12) is a sensor responsive to external stimulus.

7. The package (10) of claim 6 wherein said external stimulus is a touch.

8. A method for singulating an integrated circuit device member, the method comprising:

5 a) providing a wafer (40) containing a matrix of integrated circuit device members (44), each one of said integrated circuit device members (44) having a respective electrically active face (42) and an opposing backside (56), and a saw street (48) circumscribing each one of said integrated circuit members (44);

b) forming a trough (54) partially through said backside (56) of said wafer (40) in alignment with said saw street (48), said trough (54) having a first width; and

10 c) forming a channel (62) extending from said trough (54) to said electrically active face (54) to thereby singulate said integrated circuit device member (44), said channel (62) having a second width that is less than said first width.

15 9. The method of claim 8 wherein prior to step (b), said electrically active face (54) is non-permanently bonded to a first electrically non-conductive substrate (50).

10. The method of claim 9 wherein said non-permanent bonding is by an adhesive.

20 11. The method of claim 10 wherein said first non-conductive substrate (50) is selected to be a polymer-backed tape.

12. The method of claim 9 wherein said troughs (54) are formed to have sidewalls (58) and a base (60) with a depth of from 30% to 70% of the thickness of said integrated circuit device member (44).
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13. The method of claim 12 wherein said sidewalls (58) and said base (60) are formed to intersect at an angle of approximately 90°.

30 14. The method of claim 13 wherein said channel (62) is formed beginning at said base (60).

15. The method of claim 12 wherein prior to step (c), said wafer (40) is removed from said first non-conductive substrate (50), flipped and attached to a second non-conductive substrate with said backside (56) contacting said non-conductive substrate (50).

5 16. The method of claim 15 wherein said channel (62) is formed beginning at said saw street (48).

17. The method of claim 14 wherein following singulation said integrated circuit device (44) is removed from said non-conductive substrate (50) by a die/chip bonding pick
10 and place machine.

18. The method of claim 17 wherein said thin wafer (40) has been back-ground to a thickness of 25 microns or less.